CURRICULUM VITAE

Vladimir M. Stojanović

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Education:

03/00- 01/05 **Ph.D.** Department of Electrical Engineering, Stanford University
Advisor: Professor Mark. A. Horowitz.
Disertation topic: "Channel-Limited High-Speed Links: Modeling, Analysis and Design"
This work explores the limits of high-speed electrical signaling, imposed by channel limitations, circuit imperfections, and fundamental noise sources. Predicting system performance and identifying the worst sources of imperfections in this complex environment requires accurate statistical modeling of noise and both timing and equalization loops. Significant portion of the work is focused on analysis and adaptation of digital communication techniques to the constrained high-speed link environment. Results from two test-chips in 0.13um are reported.

09/98-03/00 **M.S.E.E.** Stanford University
Focus: Digital and Analog IC design (GPA: 4.00)

10/93-07/98 **Dipl. Ing. Diploma,** School of Electrical Engineering, University of Belgrade, Serbia
Best student in Electronics Division, class of 1998, GPA 9.65 (max. 10)
Graduate thesis: "Comparative Analysis and Modifications of MS Latches and Flip-Flops for High-Performance and Low-Power VLSI Systems"

Experience and Employment:

Academia

01/05- ***Assistant Professor***, Department of Electrical Engineering and Computer Science, Research Laboratory of Electronics, Massachusetts Institute of Technology.
Areas of interest: 1. Modeling and analysis of noise and dynamics in circuits and systems, 2. Application of optimization techniques to digital communications, analog and digital circuits, 3. High-speed electrical and optical interfaces, 5. On-chip interconnects, 6. Sensors and ultrawide-band signaling, 7. Digital communications and signal-processing architectures, 8. Clock generation and distribution, high-speed digital circuit design, VLSI and mixed-signal IC design.

03/00-09/04 ***Research Assistant***, advisor Prof. M. A. Horowitz, EE department, Stanford, University.

01/99-04/99 ***Research Assistant***, advisor Prof. M. Flynn, EE department, Stanford University
Clocking strategies in high-performance systems, skew-tolerant design and wave pipelining

10/97-04/98 ***Research Scholar***, advisor Prof. Vojin G. Oklobdžija , Advanced Computer Systems Engineering Laboratory, ECE Department, UC Davis, CA.
Comparative Analysis and Modifications of MS Latches and Flip-Flops for High-Performance and Low-Power VLSI Systems

Industry

07/01-12/04 ***Principal Engineer***, Logic Interfaces Division, Rambus Inc, Los Altos, CA
Architecture and circuit design of high-speed serial links for backplane interconnects. Design, analysis and implementation of communication techniques (coding, equalization, channel modeling/estimation). Modeling and design of clock generators and data recovery circuits.

06/99-09/99 ***Co-op position*** in Alpha processor development group, Compaq Computer Corp., Palo Alto, CA.
Circuit design of latches and flip-flops and CAD tools for their optimization and characterization.

Awards and Honors

2006 Best paper award at Signal Processing Symposium, IEEE Global Communication Conference

2006 IBM Partnership Award

2006-2007 MIT Doherty Professorship

Journal Publications:

T. Barwicz, H. Byun, F. Gan, C. W. Holzwarth, M. A. Popovic, P. T. Rakich, M. R. Watts, E. P. Ippen, F. X. Kärtner, H. I. Smith, J. S. Orcutt, R. J. Ram, V. Stojanović, O. O. Olubuyide, J. L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, and J. U. Yoon, " Silicon photonics for compact, energy-efficient interconnects [Invited]," Journal of Optical Networking, vol. 6, no. 1, pp. 63-73, 2007.

V. Stojanović, A. Ho, B.W. Garlepp, F. Chen, J. Wei, G. Tsang, E. Alon, R.T. Kollipara, C.W. Werner, J.L. Zerbe and M.A. Horowitz "Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 1012-1026, 2005.

E. Alon, V. Stojanović and M.A. Horowitz "Circuits and techniques for high-resolution measurement of on-chip power supply noise," *IEEE Journal of Solid-State Circuits,* vol. 40, no. 4, pp. 820-828, 2005.

D. Markovic, V. Stojanović, B. Nikolic, M.A. Horowitz and R.W. Brodersen "Methods for true energy-performance optimization," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 8, pp. 1282-1293, 2004.

J.L. Zerbe, C.W. Werner, V. Stojanović, F. Chen, J. Wei, G. Tsang, D. Kim, W.F. Stonecypher, A. Ho, T.P. Thrush, R.T. Kollipara, M.A. Horowitz and K.S. Donnelly "Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell," *IEEE Journal of Solid-State Circuits,* vol. 38, no. 12 SN - 0018-9200, pp. 2121-2130, 2003.

C.-K. Yang, V. Stojanović, S. Modjtahedi, M.A. Horowitz and W.F. Ellersick "A serial-link transceiver based on 8-GSamples/s A/D and D/A converters in 0.25-μm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 36, no. 11, pp. 1684-1692, 2001.

B. Nikolic, V.G. Oklobdzija, V. Stojanović, W. Jia, J.K. Chiu and M. Ming-Tak Leung "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE Journal of Solid-State Circuits,* vol. 35, no. 6, pp. 876-884, 2000.

V. Stojanović and V.G. Oklobdzija "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 4, pp. 536-548, 1999.

Conference publications

B. Kim and V. Stojanović "Equalized Interconnects for On-Chip Networks: Modeling and Optimization Framework," *IEEE International Conference on Computer-Aided Design*, Nov. 2007.

F. Chen, A. Joshi, V.Stojanović and A. Chandrakasan "Scaling and Evaluation of Carbon Nanotube Interconnects for VLSI Applications," *International Conference on Nano-Networks*, Sept. 2007.

A. Amirkhany, A. Abbasfar, V. Stojanović and M.A. Horowitz "Practical Limits of Multi-Tone Signaling Over High-Speed Backplane Electrical Links," *IEEE International Conference on Communications*, June 2007.

N. Blitvic and V. Stojanović "Statistical Simulator for Block Coded Channels with Long Residual Interference," *IEEE International Conference on Communications*, June 2007.

A. Amirkhany, A. Abbasfar, J. Savoj, M. Jeeradit, B. Garlepp, V. Stojanović, and M. Horowitz "24 Gbps, Software Programmable Multi-Channel Transmitter," *IEEE VLSI Circuits Symposium*, June 2007.

E-H. Chen, J. Ren, J.Zerbe, B. Leibowitz, H. Lee, V. Stojanović, C-K. K. Yang "BER-based Adaptation of I/O Link Equalizers," *IEEE VLSI Circuits Symposium*, June 2007.

B.S. Leibowitz, J. Kizer, H. Lee, F. Chen, A. Ho, M. Jeeradit, A. Bansal, T. Greer, S. Li, R. Farjad-Rad, W. Stonecypher, Y. Frans, B. Daly, F. Heaton, B.W. Gariepp, C.W. Werner, N. Nguyen, V. Stojanović and J.L. Zerbe "A 7.5Gb/s 10-Tap DFE Receiver with First Tap Partial Response, Spectrally Gated Adaptation, and 2nd-Order Data-Filtered CDR," *IEEE International Solid-State Circuits Conference*, pp. 228-599, Feb. 2007.

A. Amirkhany, A. Abbasfar, V. Stojanović and M.A. Horowitz, “Analog Multi-Tone Signaling for High-Speed Backplane Electrical Links,” *IEEE Global Communication Conference,* Nov 2006.

H. Hatamkhani, F. Lambrecht, V. Stojanović and C.K. Yang "Power-Centric Design of High-Speed I/Os," *ACM/IEEE Design Automation Conferenc*, pp. 867-872, 2006.

S. Vamvakos, V. Stojanović, J. Zerbe, C. Werner, D. Draper and B. Nikolic "PLL On-Chip Jitter Measurement: Analysis and Design," *IEEE VLSI Circuits Symposium,* pp. 73-74, 2006.

J. Ren, H. Lee, D. Oh, B. Leibowitz, V. Stojanovic, J. Zerbe, N. Nguyen, F. Lambrecht, Q. Lin, S. Chang, C. Yuan and V. Stojanovic "Performance Analysis of Edge-based DFE; Accurate System Voltage and Timing Margin Simulation in CDR Based High Speed Designs," *IEEE Electrical Performance of Electronic Packaging*; pp. 265; 171-268; 174, 2006.

F. Lambrecht, Q. Lin, S. Chang, D. Oh, C. Yuan and V. Stojanovic "Accurate System Voltage and Timing Margin Simulation in CDR Based High Speed Designs," *Electrical Performance of Electronic Packaging*, pp. 171-174, 2006.

C. Werner, C. Hoyer, A. Ho, M. Jeeradit, F. Chen, B. Garlepp, W. Stonecypher, S. Li, A. Bansal, A. Agarwal, E. Alon, V. Stojanović and J. Zerbe "Modeling, simulation, and design of a multi-mode 2-10 Gb/sec fully adaptive serial link system," *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, pp. 704-711, 2005.

B. Garlepp, A. Ho, V. Stojanović, F. Chen, C. Werner, G. Tsang, T. Thrush, A. Agarwal and J. Zerbe "A 1-10 Gbps PAM2, PAM4, PAM2 partial response receiver analog front end with dynamic sampler swapping capability for backplane serial communications," *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 376-379, 2005.

E. Alon, V. Stojanović, J.M. Kahn, S. Boyd and M. Horowitz "Equalization of modal dispersion in multimode fiber using spatial light modulators," *Global Telecommunications Conference, 2004. GLOBECOM '04. IEEE*, vol. 2, pp. 1023-1029, 2004.

A. Amirkhany, V. Stojanović and M.A. Horowitz "Multi-tone signaling for high-speed backplane electrical links," *Global Telecommunications Conference, 2004. GLOBECOM '04. IEEE*, vol. 2, pp. 1111-1117, 2004.

V. Stojanović, A. Amirkhany and M.A. Horowitz "Optimal linear precoding with theoretical and practical data rates in high-speed serial-link backplane communication," *Communications, 2004 IEEE International Conference on* vol. 5, pp. 2799-2806, 2004.

E. Alon, V. Stojanović and M. Horowitz "Circuits and techniques for high-resolution measurement of on-chip power supply noise," *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 102-105, 2004.

A. Ho, V. Stojanović, F. Chen, C. Werner, G. Tsang, E. Alon, R. Kollipara, J. Zerbe and M.A. Horowitz "Common-mode backchannel signaling system for differential high-speed links," *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 352-355, 2004.

V. Stojanović, A. Ho, B. Garlepp, F. Chen, J. Wei, E. Alon, C. Werner, J. Zerbe and M.A. Horowitz "Adaptive equalization and data recovery in a dual-mode (PAM2/4) serial link transceiver," *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium*, pp. 348-351, 2004.

J. Zerbe, C. Werner, V. Stojanović, F. Chen, J. Wei, G. Tsang, D. Kim, W. Stonecypher, A. Ho, T. Thrush, R. Kollipara, G.J. Yeh, M. Horowitz and K. Donnelly "Equalization and clock recovery for a 2.5-10Gb/s 2-PAM/4-PAM backplane transceiver cell," *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, pp. 80-479 vol.1, 2003.

V. Stojanović and M. Horowitz "Modeling and analysis of high-speed links," *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, pp. 589-594, 2003.

V. Stojanović, D. Marković, B. Nikolić, M.A. Horowitz and R.W. Brodersen "Energy-delay tradeoffs in combinational logic using gate sizing and supply voltage optimization," *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European*, pp. 211-214, 2002.

R.W. Brodersen, M.A. Horowitz, D. Marković, B. Nikolić and V. Stojanović "Methods for true power minimization," *Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on*, pp. 35-42, 2002.

V. Stojanović, G. Ginis and M.A. Horowitz "Transmit pre-emphasis for high-speed time-division-multiplexed serial-link transceiver," *Communications, 2002. ICC 2002. IEEE International Conference on* vol. 3, pp. 1934-1939 vol.3, 2002.

W. Ellersick, C.-K. Yang, V. Stojanović, S. Modjtahedi and M.A. Horowitz "A serial-link transceiver based on 8 GSample/s A/D and D/A converters in 0.25 μm CMOS," *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, pp. 58-59, 430, 2001.

B. Nikolić, V. Stojanovic, V.G. Oklobdžija, W. Jia, J. Chiu and M. Leung "Sense amplifier-based flip-flop," *Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International*, pp. 282-283, 1999.

V. Stojanović, V. Oklobdžija and R. Bajwa "Comparative analysis of latches and flip-flops for high-performance systems," *Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conference on*, pp. 264-269, 1998.

V. Stojanović, V.G. Oklobdžija and R. Bajwa "A unified approach in the analysis of latches and flip-flops for low-power systems," *Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on*, pp. 227-232, 1998.

Book:

V. G. Oklobdžija, V. M. Stojanović, D. M. Marković, N. M. Nedović, *Digital System Clocking: High-Performance and Low-Power Aspects*, Wiley-IEEE Press, January 2003

Patents:

V. Stojanovic, A. Ho, F. Chen, B. Garlepp “Offset cancellation in a multi-level signaling system,” United States Patent 7,233,164, issued Jun 19, 2007.

V. Stojanovic, A. Ho, A. Bessios, F. Chen, E. Alon, M. Horowitz “High Speed Signaling System with Adaptive Transmit Pre-Emphasis and Reflection Cancellation,” United States Patent 7,199,615, issued April 3, 2007.

J. Kahn, M. Horowitz, E. Alon, V. Stojanovic “Adaptive control for mitigating interference in a multimode transmission medium,“ United States Patent 7,194,155, issued March 20, 2007.

A. Ho, V. Stojanovic “Signal receiver with data precessing function,” United States Patent 7,176,721, issued February 13, 2007.

A. Amirkhany, V. Stojanovic, E. Alon, J. Zerbe, M. Horowitz “Linear Transformation Circuits,” United States Patent 7,133,463, issued November 7, 2006.

V. Stojanovic, A. Ho, A. Bessios, F. Chen, E. Alon, M. Horowitz “High Speed Signaling System with Adaptive Transmit Pre-Emphasis,” United States Patent 7,126,378, issued October 24, 2006.

E. Alon, B. Garlepp, V. Stojanovic, A. Ho, F. Chen “Circuit Calibration System and Method,” United States Patent 7,126,510, issued October 24, 2006.

V. Stojanovic “Data-level Clock Recovery,” United States Patent 7,092,472, issued August 15, 2006.

V. Stojanovic, A. Ho, A. Bessios, F. Chen, E. Alon, M. Horowitz “High Speed Signaling System with Adaptive Transmit Pre-Emphasis and Reflection Cancellation,” United States Patent 7,030,657, issued April 18, 2006.

J. L. Zerbe, V. M. Stojanovic, M. A. Horowitz, P. S. Chau “Input/output circuit with on-chip inductor to reduce parasitic capacitance,“ United States Patent 7,005,939, issued February 28, 2006.

F. F. Chen, V. Stojanović "Equalizing transceiver with reduced parasitic capacitance," United States Patent 6,982,587, issued January 3, 2006.

V. G. Oklobdžija, V. Stojanović "Flip-Flop," United States Patent 6,232,810, issued May 15, 2001.

Former Undergraduate and Graduate Advisors

Vojin G. Oklobdžija	University of Califironia Davis, Davis California and University of Belgrade, Serbia
Mark A. Horowitz	Stanford University, Stanford, California

Collaborators

Joel Dawson (MIT), Lizhong Zheng (MIT), Anantha Chandrakasan (MIT), Carl Thompson (MIT), Rajeev Ram (MIT), Judy Hoyt (MIT), Franz Kaertner (MIT), Duanne Boning (MIT), Michael Perrott (MIT), Mark Horowitz (Stanford University), Joseph Kahn (Stanford University), Stephen Boyd (Stanford University), Vojin Oklobdžija (UT Dallas), Robert Brodersen (UC Berkeley), Borivoje Nikolić (UC Berkeley), Ken Yang (UC Los Angeles), Jared Zerbe (Rambus), Peter Holloway (National Semiconductor), Jim Wieser (National Semiconductor), G. Ginis (ASSIA, Inc).

Membership in Professional Societies:

Member of IEEE (since 1996)

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